## What is claimed is:

- 1 1. A semiconductor memory device comprising:
- a memory cell area made up of a plurality of memory cells
- 3 and having an information bit area which information bits are
- 4 written in and / or read from and a parity bit area which parity
- 5 bits are written in and / or read from, and a redundant circuit
- 6 to replace error bits contained in said information bits and /
- 7 or said parity bits; and
- 8 an error correcting code (ECC) circuit to perform error
- 9 correcting processing, using a Hamming Code on data including said
- 10 information bits and said parity bits being written in and /or
- 11 read from said information bit area or said parity bit area in
- 12 said memory array; and
- wherein a combined use of redundant correcting processing
- 14 to correct said error bits using a redundant circuit in said memory
- 15 array with said error correcting processing using said Hamming
- 16 Code in said ECC circuit is made possible.
  - 1 2. The semiconductor memory device according to Claim 1,
- 2 wherein, when reading processing is performed on said information
- 3 bit area or said parity bit area, said data on which said error
- 4 correcting processing has been performed is output to only an
- 5 outside of said memory array without being rewritten into said
- 6 information bit area or said parity area.
- 1 3. The semiconductor memory device according to Claim 1,
- 2 wherein, when a codeword made up of bits occurs which is beyond
- 3 a correcting capability of said error correcting processing using

- 4 said Hamming Code, said redundant correction processing on said
- 5 error bits using said redundant circuit is made.
- 1 4. The semiconductor memory device according to Claim 1,
- 2 wherein said error correcting code (ECC) circuit comprises an
- 3 encoding circuit to output, by arithmetic operations, said parity
- 4 bit corresponding to said information bit, a decoding circuit to
- 5 output an error location detecting signal indicating an error bit
- 6 out of all bits contained in said codeword, and an error correcting
- 7 circuit to input said error location detecting signal and to
- 8 output an error bit in a reverse manner.
- 1 5. The semiconductor memory device according to Claim 4,
- 2 wherein said encoding circuit comprises a syndrome tree in which
- 3 a plurality of AND circuits to which a first test signal is fed
- 4 is connected to a plurality of exclusive OR circuits in a manner
- 5 to provide a specified relationship.
- 1 6. The semiconductor memory device according to Claim 4,
- 2 wherein said decoding circuit comprises a syndrome tree in which
- 3 a plurality of exclusive OR circuits is connected to one another
- 4 so that a plurality of bits of said information bits and a plurality
- 5 of bits of said parity bits are input and a plurality of bits of
- 6 syndromes is output and decoders to which a plurality of NAND
- 7 circuits to which a plurality of bits of said syndromes is input
- 8 and in which a plurality of bits of said error location detecting
- 9 signals are output and a plurality of AND circuits to which a second
- 10 test signal is fed are connected to one another in a manner to
- 11 provide a specified relationship.

- 1 7. The semiconductor memory device according to Claim 4,
- 2 wherein, in said error correcting circuit, a plurality of
- 3 exclusive OR circuits to which a plurality of bits of said error
- 4 location detecting signals is input together with a plurality of
- 5 bits of said information bits and a plurality of bits of said parity
- 6 bits and a plurality of switches to which a third test signal is
- 7 fed are connected to one another in a manner to provide a specified
- 8 relationship so that said error bits are output in a reverse
- 9 manner.
- 1 8. A semiconductor memory device according to Claim 1, wherein
- 2 a memory array comprising said memory cell area and said redundant
- 3 circuit.
- 1 9. A semiconductor memory device comprising:
- a memory cell area made up of a plurality of memory cells
- 3 and having an information bit area which information bits are
- 4 written in and / or read from and a parity bit area which parity
- 5 bits are written in and / or read from, and a redundant circuit
- 6 to replace error bits contained in said information bits and /
- 7 or said parity bits; and
- an error correcting code (ECC) circuit to perform error
- 9 correcting processing, using a Hamming Code whose cord length is
- 10 72 or less on data including said information bits and said parity
- 11 bits being written in and /or read from said information bit area
- 12 or said parity bit area in said memory array; and
- wherein a combined use of redundant correcting processing
- 14 to correct said error bits using a redundant circuit in said memory
- 15 array with said error correcting processing using said Hamming

- 16 Code in said ECC circuit is made possible.
  - 1 10. The semiconductor memory device according to Claim 9,
  - 2 wherein, when reading processing is performed on said information
  - 3 bit area or said parity bit area, said data on which said error
  - 4 correcting processing has been performed is output to only an
  - 5 outside of said memory array without being rewritten into said
  - 6 information bit area or said parity area.
  - 1 11. The semiconductor memory device according to Claim 9,
  - 2 wherein, when a codeword made up of bits occurs which is beyond
  - 3 a correcting capability of said error correcting processing using
  - 4 said Hamming Code, said redundant correction processing on said
  - 5 error bits using said redundant circuit is made.
  - 1 12. The semiconductor memory device according to Claim 9,
  - 2 wherein said error correcting code (ECC) circuit comprises an
  - 3 encoding circuit to output, by arithmetic operations, said parity
  - 4 bit corresponding to said information bit, a decoding circuit to
  - 5 output an error location detecting signal indicating an error bit
  - 6 out of all bits contained in said codeword, and an error correcting
  - 7 circuit to input said error location detecting signal and to
  - 8 output an error bit in a reverse manner.
  - 1 13. The semiconductor memory device according to Claim 12,
  - 2 wherein said encoding circuit comprises a syndrome tree in which
  - 3 a plurality of AND circuits to which a first test signal is fed
  - 4 is connected to a plurality of exclusive OR circuits in a manner
  - 5 to provide a specified relationship.

- 1 14. The semiconductor memory device according to Claim 12,
- 2 wherein said decoding circuit comprises a syndrome tree in which
- 3 a plurality of exclusive OR circuits is connected to one another
- 4 so that a plurality of bits of said information bits and a plurality
- 5 of bits of said parity bits are input and a plurality of bits of
- 6 syndromes is output and decoders to which a plurality of NAND
- 7 circuits to which a plurality of bits of said syndromes is input
- 8 and in which a plurality of bits of said error location detecting
- 9 signals are output and a plurality of AND circuits to which a second
- 10 test signal is fed are connected to one another in a manner to
- 11 provide a specified relationship.
- 1 15. The semiconductor memory device according to Claim 12,
- 2 wherein, in said error correcting circuit, a plurality of
- 3 exclusive OR circuits to which a plurality of bits of said error
- 4 location detecting signals is input together with a plurality of
- 5 bits of said information bits and a plurality of bits of said parity
- 6 bits and a plurality of switches to which a third test signal is
- 7 fed are connected to one another in a manner to provide a specified
- 8 relationship so that said error bits are output in a reverse
- 9 manner.
- 1 16. A semiconductor memory device according to Claim 9, wherein
- 2 a memory array comprising said memory cell area and said redundant
- 3 circuit.